What is claimed is:

1. A circuit functioning as a quadrature hybrid having an plurality of inductors and a plurality of capacitances, wherein all said capacitances are intrinsic.

2. A circuit as set forth in claim 1, comprising;

wherein said plurality of inductors comprises a first spiral inductor and a second spiral inductor;

said circuit further comprising an insulating layer disposed between said first spiral inductor and said second spiral inductor, wherein said first spiral inductor and said second spiral inductor and said insulating layer are positioned relative to each other to create an intrinsic capacitance.

3. A circuit as set forth wherein said first spiral inductor and said second spiral inductor are aligned.

4. A circuit as set forth in claim 2, further comprising:

a first output and a second output, wherein said second output is approximately ninety degrees different in phase in comparison to said first output.

5. A circuit as set forth in claim 2, wherein said first spiral inductor, said second spiral inductor, and said insulating layer are contained on a Monolithic Microwave Integrated Circuit.

6. A circuit as set forth in claim 2, wherein said insulating layer comprises Silicon Nitride.

7. A circuit as set forth in claim 2, wherein the overall length and width dimensions of said first spiral inductor and said second spiral inductor are each approximately 200 um x 200 um.

8. A circuit as set forth in claim 2, wherein the surface area of said first spiral inductor and said second spiral inductor are controlled to result in a specific intrinsic capacitance, said surface area is determined according to the following parameters:

$$C = \frac{E_o E_r A}{D}$$

where:
C= capacitance
E_o= permittivity constant of free space (equal to $8.854e^{-12}$)
E_r = dielectric constant of the insulator between the two plates
A = area of each capacitive plate
D = distance between the capacitive plates, which is equal to the thickness of the insulating layer.

9. A circuit as set forth in claim 2, wherein said first spiral inductor and said second spiral inductor each further comprise a spiral trace having a trace length, a trace width, and a spacing between the lines of said trace relative to each other,

wherein said trace length, said width, and said spacing are chosen to provide a pre-determined capacitance.

10. A circuit as set forth in claim 8, wherein said first spiral inductor and said second spiral inductor each further comprise a spiral trace having a trace length, a trace width, and a spacing between the lines of said trace relative to each other,

wherein said trace length, said width, and said spacing are chosen to provide a pre-determined capacitance.

11. A circuit as set forth in claim 2, further comprising:

a third output terminated to ground via a 50 ohm termination.

12. A circuit for performing vector modulation, said circuit encapsulated within a chip scale package, comprising:

an MMIC;

a plurality of terminating elements.

13. A circuit as set forth in claim 12, wherein said MMIC further comprises two quadrature hybrids,

wherein said hybrids comprise a first spiral inductor and a second spiral inductor;

an insulating layer disposed between said first spiral inductor and said second spiral inductor, wherein said first spiral inductor and said second spiral inductor and said insulating layer are positioned relative to each other to create an intrinsic capacitance.

14. A circuit as set forth in claim 12, wherein the size of said chip scale package is approximately 4mm x 6mm.

15. A circuit as set forth in claim 12, wherein the MMIC is comprises a layer of GaAs.

16. A circuit as set forth in claim 12, wherein the thickness of said GaAs layer is approximately equal to .004".

17. A circuit as set forth in claim 12, wherein said MMIC is configured to comprise:

an input quadrature hybrid;

a first quadrature hybrid and a second quadrature hybrid; and

an output power combiner.

18. A circuit as set forth in claim 12, wherein said input quadrature hybrid divider further comprises:

a three port power divider;

a first and a second lead/lag filter, said first filter having a leading phase shift of 45 degrees and said second filter having a lagging phase shift of 45 degrees.

19. A circuit as set forth in claim 12, wherein the terminating elements are PIN diodes.

20. A circuit as set forth in claim 12, wherein the terminating elements are Field Effect Transistors.

21. A circuit as set forth in claim 12, wherein the number of terminating elements used is equal to four.

22. A circuit as set forth in claim 12, wherein the chip scale package contains a paddle, said paddle being metallic and electrically coupled to ground.

23. A circuit as set forth in claim 12, wherein the chip scale package contains a plurality of bias pins to provide current to the diodes.

24. A circuit as set forth in claim 12, wherein the chip scale package further comprises:
an input pin for accepting a first RF signal; and,
an output pin for outputting a second RF signal, said second signal being the result of said first RF signal after the vector modulation process is performed.